REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

By the foregoing amendments, claim 2 has been canceled without prejudice or disclaimer. Claims 1, 3, 5, 26 and 38 have been amended. Thus, claims 1 and 3-39 are currently pending in the application and subject to examination.

In the Office Action mailed February 13, 2004, the Examiner rejected claims 1-39 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,108,252 to Park. It is noted that claim 2 has been canceled and that claims 1, 3, 5, 26 and 38 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

Applicants' claimed invention, as set forth in claims 1, 26 and 38, as amended, includes "a test operation mode selector circuit that, in said self-test activated condition, generates a test operation mode signal that designates any of a plurality of test operation modes including said write or read *in response to a test operation mode input signal from outside*, wherein, in response to said test operation mode signal, said test operation command generating circuit generates said test operation command for executing said test operation mode." (Emphasis added). The test operation mode of the present invention can thus be selected from the outside via *the test operation mode input signal from outside*. Therefore, it is possible to perform various operation tests by combining a plurality of test operation modes.

By contrast, Park discloses an integrated circuit memory device with self-test circuits and a method for testing the same. Specifically, Park shows a built-in self-test

("BIST") circuit, comprising a BIST portion for generating a predetermined BIST information signal. The BIST portion detects a failed address by comparing data written to the memory with data output from the memory. Park discloses stage counter 215 as designating the test operations. The test operation mode in Park, however, cannot be selected from outside. Stage counter 215 designates the test operation with a fixed order, without allowing the selection of the test operation mode from outside. *See* Park, 4:36-54. Thus, Park does not disclose or suggest at least "a test operation mode selector circuit that, in said self-test activated condition, generates a test operation mode signal that designates any of a plurality of test operation modes including said write or read *in response to a test operation mode input signal from outside*, wherein, in response to said test operation mode signal, said test operation command generating circuit generates said test operation command for executing said test operation mode," as recited in independent claims 1, 26 and 38, as amended. (Emphasis added).

For at least these reasons, Applicants submit that claims 1, 26 and 38, as amended, are allowable over the cited art. As claims 1, 26 and 38 are allowable, Applicants submit that claims 3-25, 27-37 and 39, each of which depends from claims 1, 26 or 38, are likewise allowable over the cited art.

Furthermore, Applicants' claimed invention, as set forth in claim 13, includes a "test output circuit compris[ing] a counter that counts the number of times of non-coincidence of said read data and the test data." The claimed test output circuit of the present invention outputs information regarding the number of instances of non-coincident data or the number of instances of non-coincident data, greater than a

predetermined number, after being counted by the claimed counter. Accordingly, the scale of the circuit for the claimed counter is small.

Park, by contrast, discloses clock number register 221, which stores all failure addresses and outputs all stored failure addresses. *See* Park, 4:64-67 to 5:1-10. Thus, Park does not disclose or suggest at least a "test output circuit compris[ing] a counter that counts the number of times of non-coincidence of said read data and the test data." The scale of the circuit for storing all failure addresses in Park must therefore be larger.

For at least these reasons, Applicants submit that claim 13 is allowable over the cited art. As claim 13 is allowable, Applicants submit that claims 14 and 15, each of which depends from claim 13, are likewise allowable over the cited art.

For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

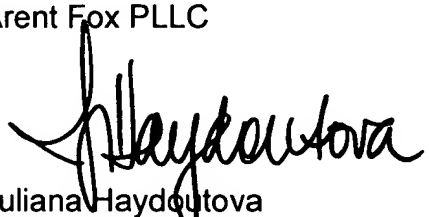
Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300, referring to client-matter number 108066-00014.

The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referring to client-matter number 108066-00014.

Respectfully submitted,

Arent Fox PLLC



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Enclosure: Petition for Extension of Time (one month)

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